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# A REVIWE ARTICLE OF FPGA DESIGN FUNDAMENTAL AND SERIAL COMMUNICATION TECHNIQUE

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## ABSTRACT

Communication and interoperation are critical to modern industry. A reconfigurable intelligent gateway based on ARM and FPGA is proposed on the basis of current situation and developing trend of protocol converting to achieve communication and interoperation among heterogeneous field bus systems and TCP/IP network. The functional block diagram, hardware architecture, software structure and protocol converting and communication model of the gateway are presented. The proposed gateway has a strong intelligent control ability, flexibility, reliability, fast conversion speed, consolidated device description and upper-level interface. It can also be updated online, and used as protocol converter or stand-alone intelligent controller, and has great theoretical significance and practical value in the field of heterogeneous networks communication and interoperation.

**KEYWORDS**: communication, interoperation, protocol converting, reconfigurable gateway.

## I. INTRODUCTION

A **field-programmable gate array** (**FPGA**) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). (Circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare.)

A Spartan FPGA from Xilinx FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.


***Fig(1) FPGA IC***

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## II. DESIGNING FUDAMENTALS WORK

Contemporary field-programmable gate arrays (FPGAs) have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fast I/Os and bidirectional data buses, it becomes a challenge to verify correct timing of valid data within setup time and hold time. Floor planning enables resources allocation within FPGAs to meet these time constraints. FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design[2] and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications.

Some FPGAs have analog features in addition to digital functions. The most common analog feature is programmable slew rate on each output pin, allowing the engineer to set low rates on lightly loaded pins that would otherwise ring or couple unacceptably, and to set higher rates on heavily loaded pins on high-speed channels that would otherwise run too slowly.[3][4] Also common are quartz-crystal oscillators, on-chip resistance-capacitance oscillators, and phase-locked loops with embedded voltage-controlled oscillators used for clock generation and management and for high-speed serializer- deserializer (SERDES) transmit clocks and receiver clock recovery. Fairly common are differential comparators on input pins designed to be connected to differential signaling channels. A few "mixed signal FPGAs" have integrated peripheral analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip.[5] Such devices blur the line between an FPGA, which carries digital ones and zeros on its internal programmable interconnect fabric, and field-programmable analog array (FPAA), which carries analog values on its internal programmable interconnect fabric.

In order to reduce time-to-market, power consumption and product costs while improving product quality and efficiency, industrial companies face many challenges. One of these challenges is enhancing collaborative and integrated production automation, which requires close interoperability among various sub-systems. Interoperability can be defined as the ability of two systems or more to communicate cooperate and exchange data and services, despite differences in languages, implementations and executive environments or abstract models [1]. The basis of interoperation is smooth and real-time communication.

In the areas of manufacturing, building automation, power and energy plants and logistics, the modern automation systems are wildly used which have very often a distributed nature. The control system is consist of a large number of control, measurement and field devices, in order to achieve the good control effect the communication and interoperation among all the devices is a critical factor. Today, a trend towards the usage of Ethernet-based approaches can be observed providing a common hardware communication standard in the a fore mentioned applications areas.

The vision of only using one hardware and software standard covering all communication needs and requirements in industrial-process measurement, control, and automation systems is still a high-level goal and a nearly unreachable challenge in real-world applications so far [4]. For example, the field-buses varied from protocol, data format, structure, media, application field, etc.. So they cannot communicate to each other directly, not to mention the interoperability. In order to solve this problem, gateway and middleware are used to perform protocol converting among heterogeneous field bus networks.

## III. PROTOCOL CONVERTING GATEWAY:

In general, field bus protocol is based on ISO/OSI Open Systems Interconnection model. A typical field bus protocol contains physical layer, data link layer, th network layer, application layer and user layer. Each field bus has its own definition of the layers, so the protocol conversion is taken place mainly on data link layer, application layer and user layer by a MCU+ASIC architecture gateway [5], which is illustrated in Figure 1. The MCU+ASIC protocol converting gateway has simple structure and easy to be implemented. It can convert protocol among field bus A, field bus B and Ethernet. The ASIC contains the physical layer and data link layer, is the bottom-level data transceiver. The MCU is the application layer and user layer, complete the data mapping and format conversion [6]. This kind of gateway is widely used in the industrial automatic control. However, the following deficiencies are also exposed in practical applications.

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- Poor expansibility and upgrade ability. If the protocol was changed during the field equipment upgrade, or a new sensor and actuator with different protocol was added into the network, the gateway would lose its functions.

- Limited processing capacity. In some kind of broadcast network, the irrelevant data should be filtered on the bottom layer, but the data was processed on the upper layer in existing gateway which impairs the system's processing power and real-time performance.

- Lack of control ability. In order to reduce the communication and ensure the real-time performance of large distributed system, data preprocessing and some simple control function should performed on the field, while the existing gateway is without this ability

**Interconnection Middleware**

The middleware has standard communication interface and protocol, and is used in some heterogeneous network interconnection [7,8]. Regardless of the change and update of bottom layer system software, as long as the middleware was updated and the interface remained unchanged, the upper software can remain unchanged. The existing heterogeneous network interconnection middleware is mainly based on OPC, DDE and ODBC, etc, Figure 2 is the middleware module based on OPC interface. However the middleware can not satisfy the real-time performance and data security requirements, and lacks bottom layer hardware support [9].

**Objectives of project**

Through the above analysis, we can see that the off-shelf gateway and middleware are insufficient in terms of intelligence, flexibility, online update, real-time performance, control ability, etc. with the constantly emerging of new control technology, sensors and actuators.

In this context, we have developed an innovative reconfigurable intelligent gateway based on ARM and FPGA to achieve heterogeneous networks communication and interoperability which combining the advantages of current protocol converting gateway and middleware, and has better intelligence, flexibility, scalability. Therefore, the paper is organized as follows: Section 2 presents the architecture, protocol converting and communication model of the proposed reconfigurable intelligent gateway. Section 3 describes an implementation of the gateway, several tests in detail, and research prospects. Finally, Section 4 will conclude the paper.

## IV. ISSUE OF PREVIOUS ARTICLES

### 1. Jaskirat Kaur1

Xilinx ISE (Integrated Software Environment) is a software tool manufactured by Xilinx for synthesis and analysis of HDL designs. Xilinx tools are capable of designing digital circuits using Field Programmable Gate Array (FPGA). Field-Programmable Gate Arrays (FPGAs) are specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. FPGAs offer more narrow logic resources in comparison to CPLDs feature logic resources with a wide number of inputs (AND planes). The objective of this paper is to describe how Xilinx tools and FPGA families are used to amend digital designs. In this paper we are also describing how different types of FSM are assistance in the designing of digital hardware.

### 2. Rajdeep Chakraborty

In this paper a block cipher based new cryptosystem has been proposed, where the encryption is done through Triangular Modulo Arithmetic Technique (TMAT), which consists of three phases. The original message is considered as a stream of bits. In Phase 1, bit stream is divided into a number of equal size blocks. Then the Triangular algorithm is performed on odd blocks, where even blocks are remain unchanged and together form a bit stream. In Phase 2, MAT is performed on that bit stream, which is divided into a number of blocks, each containing n bits, n is 2k,, k is 1, 2, 3 and so on. Then modulo addition is performed between first and second block and the content of the second block is replaced by the result, where the first block is remain unchanged. This is continuing till the last block is changed and also for block size n is 2, 4, 8, and so on. In case of modulo addition the carry out of the MSB is discarded. In Phase 3, the Triangular algorithm is performed on even blocks but odd blocks are remain unchanged and together form output stream.

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**3. M. Dhruvakumar**

Wireless technology is emerged has the vibrant research areas in the modern communication industry. The IEEE 802.16e has defined a standard called mobile WiMAX and emerged as the latest wireless technology that has promised to offer Broadband Wireless Access over long distance. The OFDM technique is used in WiMAX to obtain high data rate in addition to reducing the effects of inter symbol interference and inter channel interference. This paper proposes an algorithm to model the Address Generation circuitry of WiMAX Deinterleaver using Verilog on FPGA platform with all code rates and modulation schemes of IEEE 802.16e standard. The implementation of floor function in FPGA is very difficult in IEEE 802.16e standard. Hence the requirement of floor function can be eliminated by using a simple mathematical algorithm. The main scope of the work is to concentrate on performance improvement by reducing interconnection delay, lesser power consumption, and efficient resource utilization by comparing with prevailing technique.

This paper proposes a novel algorithm including proof for address generation circuitry of the WiMAX channel deinter leaver supporting QPSK and 16-QAM modulation patterns and all possible code rates as per IEEE 802.16e. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA using Verilog. Comparison of our proposed work with a conventional LUT-based method and also with a recent work show significant improvement on resource utilization and operating frequency.

## V. MANUFACTURING OF FPGA

In the late 1980s, the Naval Surface Warfare Center funded an experiment proposed by Steve Cassel man to develop a computer that would implement 600,000 reprogrammable gates. Cassel man was successful and a patent related to the system was issued in 1992.[6]

Some of the industry's foundational concepts and technologies for programmable logic arrays, gates, and logic blocks are founded in patents awarded to David W. Page and LuVerne R. Peterson in 1985.[7][8]

Altera was founded in 1983 and delivered the industry's first reprogrammable logic device in 1984 – the EP300 – which featured a quartz window in the package that allowed users to shine an ultra-violet lamp on the die to erase the EPROM cells that held the device configuration.[9]

Xilinx co-founders Ross Freeman and Bernard Vonder schmitt invented the first commercially viable field-programmable gate array in 1985 – the XC2064.[10][11][*not in citation given*]The XC2064 had programmable gates and programmable interconnects between gates, the beginnings of a new technology and market.[12] The XC2064 had 64 configurable logic blocks (CLBs), with two three-input lookup tables (LUTs).[13] More than 20 years later, Freeman was entered into the National Inventors Hall of Fame for his invention.[14][15]

Altera and Xilinx continued unchallenged and quickly grew from 1985 to the mid-1990s, when competitors sprouted up, eroding significant market share. By 1993, Actel (nowMicrosemi) was serving about 18 percent of the market.[12] By 2010, Altera (31 percent), Actel (10 percent) and Xilinx (36 percent) together represented approximately 77 percent of the FPGA market.[16]

The 1990s were an explosive period of time for FPGAs, both in sophistication and the volume of production. In the early 1990s, FPGAs were primarily used in telecommunications and networking. By the end of the decade, FPGAs found their way into consumer, automotive, and industrial applications.

Xilinx and Altera are the current FPGA market leaders and long-time industry rivals. Together, they control over 80 percent of the market.[44] Both Xilinx and Altera provide proprietary Windows and Linux design software (ISE/Vivado and Quartus) which enable engineers to design, analyze, simulate and synthesize (compile) their designs.
Other manufacturers include:

Lattice Semiconductor (SRAM based with integrated configuration flash, instant-on, low power, live reconfiguration) Microsemi (previously Actel, antifuse, flash-based, mixed-signal)

Silicon Blue Technologies (extremely low power SRAM-based FPGAs with optional integrated nonvolatile configuration memory; acquired by Lattice in 2011) Achronix (SRAM based, 1.5 GHz fabric speed), Quick

Logic (Ultra Low Power Sensor Hubs, extremely low powered, low density SRAM-based FPGAs, Display bridges MIPI & RGB inputs, MIPI, RGB and LVDS outputs) e2v (previously QP semiconductor) Atmel (second source of some Altera-compatible devices; also FPSLIC mentioned above) . In March 2010, Tabula announced their FPGA technology that uses time-multiplexed logic and interconnect that claims potential cost savings for high-density applications.[49] On March 24, 2015, Tabula officially shut down.[50]
On June 1, 2015, Intel announced it would acquire Altera for approximately $16.7 billion and completed the acquisition on December

## VI. METHODOLOGY AND SOFTWARE

### i. VHDL (Very High speed integrated Hardware Description Language):

VHDL is abbreviation of VHSIC (very high-speed integrated circuits program) and Hardware Description Language. It is used for the purpose of buildings accurate model of complex digital system. VHDL is a programming language for designing and modeling digital hardware systems. VHDL allow electrical aspects of circuit behavior to be precisely described. VHDL though being a rigid language with a standard set of rules allows the designer to use different methods of design giving different technique to represent the digital system. The most important applications of VHDL are to capture the performance specification for a circuit, in the form of a test bench. Test benches a descriptions of circuit expected outputs that verify the behavior of a circuit over time. Test benches are integral part of any VHDL project and should be created with other descriptions of the circuit.[2] The reason why we use VHDL is that it increases the productivity and rapid speed of development in electronic design automation (EDA) tools and in target technologies. VHDL models are based on the process of inference. Inference is ensued by optimization of to reduce size or increase the pace of the circuits re VHDL .

### ii. Finite State Machines

FSM is basically a sequential system. It comprises internal stages. FSM is reckoning model for both software and hardware. Finite state machines (FSM) are a basic component in hardware design; they represent the transformation between inputs and outputs for sequential designs[3].Synchronous FSM and Asynchronous FSM are distinct concept or state of exchanging information between entities. Synchronous FSM having clock and its state can change value only at a triggering clock edge. Communication and computations occurs instantly at discrete time. It may be difficult to design. However, in asynchronous FSM there is no clock and its state can change value when its input value changes. They are free to proceed independently and do not execute a transition at same time. Implementation of asynchronous FSM is easy. They can operate faster and use less power as compared to synchronous FSM.

***Moore versus Mealy Machines***

In Moore FSM, output is function of only its present state .The outputs of Moore FSM can change only at a triggering clock edge. However in MEALY FSM, output is function of both its input and its present state. The output of Mealy FSM can change as soon as any of its input changes.[4] The advantage of Moore model is a simplification of the

### iii. Field programmable gate array (FPGA)

Field Programmable Gate Arrays are absolute new intellect class of integrated circuit. It was introduced by the Xilinx Company in 1985. FPGA are digital logic chips that can be reconfigured so that they perform logic functions [7]. The basic architecture of FPGA comprises a logic blocks and interconnections between logic blocks and input /output blocks (IOBs).Hardware description language such as VHDL is used to describe FPGA configurations. It can integrate large amount of simple data paths and random logics. FPGA can be easily reprogrammed to reflect changes in system components [4]. FPGA having flexible interconnect continuous routing structure for fast, predictable interconnect delays. [16]. although a wide range of architectures is available, generally an FPGA consists of an *NxN* array of programmable logical units (LUs) and programmable I/O blocks, connected by a programmable interconnection network [8].

Purpose of Xilinx AND MATLAB tools: Xilinx is a Synthesis Tool which converts Schematic/HDL Design Entry into functionally equivalent logic gates on Xilinx FPGA, with optimized speed & area. So, after specifying behavioral description for HDL, the designer merely has to select the Library and specify Optimization Criteria; and Xilinx Synthesis Tool determines the netlist to meet the framing. After that it is then converted into Bit-File and to be loaded onto FPGA [12]. Also, Xilinx Tool generates Post-Process Simulation Model after every Implementation Step, which is used to functionally verify generated netlist after processes,

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like Place & Route. Xilinx allows Mixed Mode HDL Design Entry. Xilinx productivity advantage helps in efficiently migrate FPGA designs to hardware platform [13].

## VII. ADVANTAGE OF PROPOSED METHODE

**Device Utilization Summary on FPGA:** Table no. 1 shows the Design Summary of the I2C single master**.** The result shows that minimal resources are utilized in designing the I2C master as only 3% slices, 0% flip flops and 2% LUTs are utilized.

Historically, FPGAs have been slower, less energy efficient and generally achieved less functionality than their fixed ASIC counterparts. An older study had shown that designs implemented on FPGAs need on average 40 times as much area, draw 12 times as much dynamic power, and run at one third the speed of corresponding ASIC implementations[*citation needed*]. More recently, FPGAs such as the Xilinx Virtex-7 or the Altera Stratix 5 have come to rival corresponding ASIC and ASSP solutions by providing significantly reduced power, increased speed, lower materials cost, minimal implementation real-estate, and increased possibilities for re-configuration 'on-the-fly'. Where previously a design may have included 6 to 10 ASICs, the same design can now be achieved using only one FPGA.

## VIII. CONCLUSION & FUTURE SCOPE

CMOS Single Master is successfully designed using Verilog, simulated in Modelsim and synthesized using Xilinx. As the number of devices connected to a system is going to increase, there is a need for a system which supports multiple protocols. This project can be further extended to design for multiple masters.

An FPGA can be used to solve any problem which is computable. This is trivially proven by the fact FPGA can be used to implement a soft microprocessor, such as the Xilinx MicroBlaze or Altera Nios II. Their advantage lies in that they are sometimes significantly faster for some applications because of their parallel nature and optimality in terms of the number of gates used for a certain process.

Specific applications of FPGAs include digital signal processing, software-defined radio, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, Bioinformatics, computer hardware emulation, radio astronomy, metal detection and a growing range of other areas.

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